Seat No.

Total No. of Pages: 3

OCT_NOV_2024 WINTER EXAMINATION

12329 Bachelor of Computer Application(BCAsci) NEP 2.0

Sub. Name: Computer Architecture

	Sub. Code: 109808		
Down	I Date: FEBRUARY ,17-02-2025	A + 8 = 8 + A A	
		Total Marks: 60	
	0:30 AM To 12:30 PM	C. A • (B • C) = (A • B) • C	
Instruc	tions: 1. Figures to the right indicate full marks	D. A + B = B + A	
Special			
	2) Attempt any THREE questions from Que		
affected by		A. To count wo of by chang	
Q1) S	olve following MCQ.	tore a storoT .[10]	
172329) 1	sick storof Computer Application (NERGO) is the sister	Archiverfields ad Sonta O	
l.	Convert binary to octal: (110110001010)2	D, Error Detaction	
	A. (5512)8		
		ix. Whose operations are with a faster	
	C. (4532)8	A. Combinational circles	
	D. (4130)8	B. Sequential circuits	
	The desired and also to the desired	-C. Latches	
II.	The decimal equivalent of the binary number (101	(1.011)2 is eqoff-qiF .Q	
	A. (11.175)10		
		x. Which memory has largest storage	
	C. (10.123)10	A. Auxiliary memory	
	D. (9.23)10	B. RAM	
III.	The gates required to build a helf adder are	C. Associative memory	
III.	The gates required to build a half adder are A. EX OR Gate And AND Gate	D Cache memory	
	B. EX-OR Gate And OR Gate	32) What are logic gates? Explain dillera	
	C. EX-NOR Gate And AND Gate		
	D. EX-OR Gate And NOR Gate	diagram.	
		23) What is Flip flops? Explain SR and D fl	
iv.	2's complement of binary number 0101 is	to a series of the series of t	
		24) What is (aumaugh map (K' Map)? Wh	
	B. 1111		
	Inumber system and with sulfable exertion .0 In	25) Explain Binary, Octal and Hexadecima	
	nary, Octal and Hexadecimal? 0111 .d	number conversion from Decimal to Bir	
	5. 1110		
v.	In boolean algebra, the OR operation is performed	d by which properties?	
	A. Associative Properties		
	B. Commutative Properties	(Arry Four out of Six)	
	C. Distributive Properties		
	D. All Of Above	SOP bits 908	
	ran	anh and I by wheel and I	
vi.	The gates required to build a half adder are	b. Decoders and Encoder	

Q2)

Q3)

Q4)

Q5)

Q6)

Q7)

SOP and POS

Decoders and Encoder

[2]

e gates required to build a half adder are

. C.	Half Adder and Full Adder	<i>QP-3258</i> [5]
d.	Program Counter and Accumulator registers	[5]
e.	DeMorgan Laws	[5]
f.	Shift registers	[5]

End Of Question Paper

Important Note for Chief Exam Officer / SRPD Coordinator / Sr Supervisor/ Student - This Question Paper may be distributed for following Subjects as common code. सदरची प्रश्नपत्रिका खालील विषयांकरिता वितरित करता येईल.

1] (12329) Bachelor Of Computer Application (NEP2.0) (109808) Computer Architecture Part 1 SEM 1